Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L19	controller near6 writ$3 same (clear data or color pixel) same (bank or subregion or sub-region or subsection or sub-section)	1	L19
L18	clear data near6 (parallel or concurren$4 or simultan$6) same controller	1	L18
L17	controller same writ$3 same (clear data or color pixel) same (bank or subregion or sub-region or subsection or sub-section)	10	L17
L16	controller adj3 writ$3 adj8 (clear data or color pixel) adj4 (bank or subregion or sub-region or subsection or sub-section)	0	L16
L15	L12 same (parallel or concurren$4 or simultan$6)	9	L15
L14	(parallel or concurren$4 or simultan$6) near3 clear data same memory	5	L14
L13	clear adj2 data same controller same memory near3 (subregion or sub-region or subsection or sub-section)	0	L13
L12	clear adj2 data same controller same memory	192	L12
L11	L7 and memory near3 (subregion or sub-region or subsection or sub-section)	0	L11
L10	L8 and memory near3 (subregion or sub-region or subsection or sub-section)	0	L10
L9	L8 same (subregion or sub-region or subsection or sub-section)	0	L9
L8	L7 same memory	54	L8
L7	clear near2 data near5 controller	124	L7
L6	L5 same controller	4	L6
L5	L2 not l4	41	L5
L4	L2 and((clear near3 data) or (color near3 pixel))	4	L4
L3	L2 same ((clear near3 data) or (color near3 pixel))	0	L3
L2	L1	45	L2
	DB=USPT; PLUR=YES; OP=ADJ		
L1	memory adj2 (region or section) adj5 (subregion or sub-region or subsection or sub-section)	45	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6321266 B1

L17: Entry 1 of 10 File: USPT Nov 20, 2001

DOCUMENT-IDENTIFIER: US 6321266 B1
**** See image for Certificate of Correction ****
TITLE: Input/output apparatus connected to a plurality of host computers via a network

Detailed Description Text (66):
Though there are usually several kinds of methods for accessing DRAMs; a method for accessing word (8, 16, 32, - - - bits) by word; a method for accessing serially with a predetermined bit length (page READ, Write); and an interleave method in which divided DRAM banks are alternatively accessed and addresses are generated in advance, all the above methods can be applied so as to speed up the memory access. When the main memory 102 and the band memory 103 are constituted of SRAMs, it is not required to refresh. A memory clear controller 105 clears the data in the band memory 103 in a high speed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 2. Document ID: US 6177934 B1

L17: Entry 2 of 10 File: USPT Jan 23, 2001

DOCUMENT-IDENTIFIER: US 6177934 B1
**** See image for Certificate of Correction ****
TITLE: Server device and image processing device

Detailed Description Text (66):
Though there are usually several kinds of methods for accessing DRAMS; a method for accessing word (8, 16, 32, - - - bits) by word; a method for accessing serially with a predetermined bit length (page READ, Write); and an interleave method in which divided DRAM banks are alternatively accessed and addresses are generated in advance, all the above methods can be applied so as to speed up the memory access. When the main memory 102 and the band memory 103 are constituted of SRAMs, it is not required to refresh. A memory clear controller 105 clears the data in the band memory 103 in a high speed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 5996029 A

L17: Entry 3 of 10 File: USPT Nov 30, 1999

DOCUMENT-IDENTIFIER: US 5996029 A
**** See image for Certificate of Correction ****

TITLE: Information input/output control apparatus and method for indicating which of at least one information terminal device is able to execute a functional operation based on environmental information

Detailed Description Text (66):
Though there are usually several kinds of methods for accessing DRAMs; a method for accessing word (8, 16, 32, . . . bits) by word; a method for accessing serially with a predetermined bit length (page READ, Write); and an interleave method in which divided DRAM banks are alternatively accessed and addresses are generated in advance, all the above methods can be applied so as to speed up the memory access. When the main memory 102 and the band memory 103 are constituted of SRAMs, it is not required to refresh. A memory clear controller 105 clears the data in the band memory 103 in a high speed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5859956 A

L17: Entry 4 of 10 File: USPT Jan 12, 1999

DOCUMENT-IDENTIFIER: US 5859956 A
**** See image for Certificate of Correction ****
TITLE: Information processing device and information processing method

Detailed Description Text (66):
Though there are usually several kinds of methods for accessing DRAMs; a method for accessing word (8, 16, 32, - - - bits) by word; a method for accessing serially with a predetermined bit length (page READ, Write); and an interleave method in which divided DRAM banks are alternatively accessed and addresses are generated in advance, all the above methods can be applied so as to speed up the memory access. When the main memory 102 and the band memory 103 are constituted of SRAMs, it is not required to refresh. A memory clear controller 105 clears the data in the band memory 103 in a high speed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 5793386 A

L17: Entry 5 of 10 File: USPT Aug 11, 1998

DOCUMENT-IDENTIFIER: US 5793386 A
TITLE: Register set reordering for a graphics processor based upon the type of primitive to be rendered

Detailed Description Text (6):
Referring still to FIG. 1, the graphics processor 100 preferably couples to the system bus 25. In accordance with the preferred embodiment, the graphics processor 100 preferably includes bus mastering capabilities, thus permitting graphics processor 100 to obtain mastership of the system bus 25. By obtaining mastership of the system bus, the graphics processor 100 can read the display list from system memory 75, instead of waiting until the host processor performs a write operation. This mode of operation is called the "processor mode." As shown in FIG. 1, graphics controller 100 also connects to a display unit 60 and a RDRAM 85. In the preferred embodiment, the RDRAM 85 comprises a bank of RDRAM buffers, where the digital data stored in the RDRAM comprises a rectangular array of picture elements referred to as pixels or pixel values. Each pixel can be defined by an 8 bit value, for example, which specifies the intensity of a single color of a corresponding pixel on a screen of the display unit 60. For full

color display, either three passes are made or three parallel logic slices are implemented for the three primary colors to achieve 24 bit pixel values. The display unit 60 may be any suitable type of display device, such as a cathode ray tube (CRT) for desktop, workstation or server applications, a liquid crystal display (LCD), a thin film transistor (TFT) display, or any other suitable display device for a personal computer.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

6. Document ID: US 5740028 A

L17: Entry 6 of 10 File: USPT Apr 14, 1998

DOCUMENT-IDENTIFIER: US 5740028 A
**** See image for Certificate of Correction ****
TITLE: Information input/output control device and method therefor

Detailed Description Text (66):
Though there are usually several kinds of methods for accessing DRAMs; a method for accessing word (8, 16, 32, --bits) by word; a method for accessing serially with a predetermined bit length (page READ, Write); and an interleave method in which divided DRAM banks are alternatively accessed and addresses are generated in advance, all the above methods can be applied so as to speed up the memory access. When the main memory 102 and the band memory 103 are constituted of SRAMs, it is not required to refresh. A memory clear controller 105 clears the data in the band memory 103 in a high speed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

7. Document ID: US 5613147 A

L17: Entry 7 of 10 File: USPT Mar 18, 1997

DOCUMENT-IDENTIFIER: US 5613147 A
TITLE: Signal processor having a delay ram for generating sound effects

Detailed Description Text (39):
On the other hand, upon receiving the memory clear command CLR1, the delaying address controller 12 clears the data written into the memory bank 4.sub.1 of the delay RAM 4, as will be described in detail hereinbelow. Further, the CPU 2 periodically makes a check as to whether or not the clear enable signal CLE1 is in the logical state "0" When the clear enable signal is in the logical state "0", it is judged that clearing of the memory bank 4.sub.1 of the delay RAM 4 has been completed, and then the muting of the output level of the effecter block EF1 is canceled, whereby the output level of the effecter block EF1 for pitch change progressively increases immediately after canceling of the muting, as shown in FIG. 9.

Detailed Description Text (44):
Then, the modified address data MAD is delivered to the memory controller 13 appearing in FIG. 8. In the present case, the memory controller 13 is supplied with the memory clear signal MCLR, and accordingly, both the selectors 39 and 40 select the data of "0" input thereto via their input terminals B and supply the data of "0" to the delay RAM 4 through the data input terminal DTA and the write/read control terminal NW/R, respectively. For the first clock .phi. after starting the memory clear, the data of "0" is written into the ending address (TAD2-1) of the area 4.sub.1 of the delay RAM 4, in other words, the musical tone data of the ending address (TAD2-1) of the memory bank 4.sub.1 of the delay RAM 4 is cleared.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

8. Document ID: US 5422657 A

L17: Entry 8 of 10 File: USPT Jun 6, 1995

DOCUMENT-IDENTIFIER: US 5422657 A
TITLE: Graphics memory architecture for multimode display system

Detailed Description Text (9):
The graphics memory controller 403 outputs pixels to be transmitted to the frame memory 500 via the bus 402 and written into the frame memory 500. The graphics memory controller 403 includes a pixel output swap circuit 90. The pixel output swap circuit 90 receives true color pixels whose R, G and B components are located in the first three bytes of a four byte word and rearranges the R, G and B components so that the pixel may be written into a particular bank in the memory 500. For index color pixels, the pixel output swap circuit 90 receives four consecutive index color pixels in a four byte word and reorders the index color pixels so they may be written into one of the three (R,G or B) index color buffers in the memory 500.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

9. Document ID: US 3833887 A

L17: Entry 9 of 10 File: USPT Sep 3, 1974

DOCUMENT-IDENTIFIER: US 3833887 A
TITLE: PROGRAMMABLE CONTROLLER

Brief Summary Text (7):
The controller is a programmable, solid-state digital computer, designed primarily for input/output operations required in controlling electromechanical devices or communications devices. The system is a single-address, 16-bit computer using 2's complement arithmetic. The memory system is 16-bit word oriented; the memory banks each have a capacity of 4,096 16-bit words. The use of two 4K x 8 memory units to construct each bank facilitates the retrieval or storage of either the most significant byte or the least significant byte, the other byte being left in memory unchanged. Each instruction occupies two bytes (one in the upper half of the memory bank, the other in the lower half); any 16-bit instruction or data word can be accessed by a 12-bit address that is supplied simultaneously to both memory units of both banks. The Address Reset signal sets the address into all four memory address registers and clears the data registers; however, Initiate Read and Initiate Write commands are supplied only to one bank at a time, under program control. Execution of instructions requires 2 microseconds for the Fetch sequence and between 1 and 16 microseconds for the Execute sequence; the average execution time for instructions other than Shift or Rotate is 5 microseconds. A single interrupt channel is provided and is shared by the paper tape punch and the Selectric and Auxiliary keyboards; when an interrupt request is granted, control is transferred to a predetermined memory location, where a servicing routine identifies the interrupting device and takes the required action.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 10. Document ID: US 3731280 A

L17: Entry 10 of 10 File: USPT May 1, 1973

DOCUMENT-IDENTIFIER: US 3731280 A
TITLE: PROGRAMMABLE CONTROLLER

Brief Summary Text (7):
The controller is a programmable, solid-state digital computer, designed primarily for input/output operations required in controlling electromechanical devices or communications devices. The system is a single-address, 16-bit computer using 2's complement arithmetic. The memory system is 16-bit word oriented; the memory banks each have a capacity of 4096 16-bit words. The use of two 4K .times.8 memory units to construct each bank facilitates the retrieval or storage of either the most significant byte or the least significant byte, the other byte being left in memory unchanged. Each instruction occupies two bytes (one in the upper half of the memory bank, the other in the lower half); any 16-bit instruction or data word can be accessed by a 12-bit address that is supplied simultaneously to both memory units of both banks. The Address Reset signal sets the address into all four memory address registers and clears the data registers; however, Initiate Read and Initiate Write commands are supplied only to one bank at a time, under program control. Execution of instructions requires 2 microseconds for the Fetch sequence and between 1 and 16 microseconds for the Execute sequence; the average execution time for instructions other than Shift or Rotate is 5 microseconds. A single interrupt channel is provided and is shared by the paper tape punch and the Selectric and Auxiliary keyboards; when an interrupt request is granted, control is transferred to a predetermined memory location, where a servicing routine identifies the interrupting device and takes the required action.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

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Terms	Documents
controller same writ$3 same (clear data or color pixel) same (bank or subregion or sub-region or subsection or sub-section)	10

Display Format: - Change Format

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☐ 1. Document ID: US 6459500 B1

L4: Entry 1 of 4 File: USPT Oct 1, 2002

DOCUMENT-IDENTIFIER: US 6459500 B1
TITLE: Image processing apparatus

Brief Summary Text (28):
Meanwhile, the characteristic amounts include a dynamic range, an average density, a pixel density distribution, a color balance of a highlight region, a color balance of a middle density region and a color balance of a shadow region and the like.

Detailed Description Text (50):
At first, in the step 100 in FIG. 3, the prescanned image is read out from the prescan memory 40 into the region extracting subsection 50 of the display image processing section 44. In the next step 110, a principal subject region such as a human individual and the like is extracted form the thus read-out prescanned image so that the principal subject region and the background region are divided from each other. As described above, this division is executed either automatically or by performing an auxiliary inputting operation by an operator.

Detailed Description Text (62):
In the first place, an image data for analyzing the principal subject region is formed by multiplying prescanned image data read out from the prescan memory 40 into the color reproduction parameter forming section 48 by the weight of the unsharp weighting image. The color reproduction parameter, that is, correction gradation, is calculated from characteristic amounts such as dynamic range, average density value, pixel density distribution, color balances of a highlight portion, a middle portion, a shadow portion and the like. Alternatively, color reproduction parameter of the principal subject region, that is, correction gradation, may be inputted from the auxiliary inputting section 78 by an operator. A correction amount obtained by multiplying the thus obtained correction gradation by the weight of the unsharp weighting image is set in the second LUT 76 as a color reproduction parameter of the principal subject region. This correction amount comprises R, G and B signals, a luminance signal or both, and these signals are to be added to the image data signal.

CLAIMS:

9. The image processing apparatus according to claim 7, wherein said characteristic amounts include at least one of a dynamic range, an average density, a pixel density distribution, a color balance of a highlight region, a color balance of a middle density region and a color balance of a shadow region.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments   KWIC | Draw Desc | Image

☐ 2. Document ID: US 5754186 A

L4: Entry 2 of 4 File: USPT May 19, 1998

DOCUMENT-IDENTIFIER: US 5754186 A
TITLE: Method and apparatus for blending images

Brief Summary Text (15):
The invention provides for the blending of first and second images loaded into corresponding VRAM buffers. The first and second images may, for example, be opaque and translucent images or windows displayed on a computer display screen. According to the invention, the blending of image data is effective for producing a combined image on the display screen of a computer screen assembly by first storing respective first and second images, such as for example, video and overlay images, in corresponding first and second VRAM buffers, combining pixel amounts thereof in a blending operation which combines nibble or byte contributions from each of the images to be blended, and addressing a preestablished look-up table in a CSC chip in order to establish the character of single pixel presentation on a computer screen. The VRAM buffer is loaded byte by byte, each byte comprising first and second nibbles representing image contributions for successive pixels "A" and "B." As a result of the indicated information scheduling activity, the first image information on a particular pixel will be in a particular one of the VRAM buffers and the corresponding second video information, i.e., the overlay information, is in the other VRAM buffer. After completion of blending operation, the CSC chip is called for addressing a color or gray scale look up table fabricated as part of the video driver circuitry. The color look-up table is a preferred version of the invention in which the color look-up table controls the color in pixels within a selected frame being displayed on a computer screen. According to an alternate embodiment of the invention, gray scale information is selected by the blending output to produce frame pixel information for presentation on a computer screen.

Drawing Description Text (11):
FIG. 9 illustrates features of a CSC chip which includes a color look-up table according to a preferred version of the invention in which the color look-up table controls the color in pixels within an image frame being displayed on a computer screen; and

Detailed Description Text (19):
VRAM loading and image blending process according to the invention is conducted as follows. First, buffers 308 and 310 are initialized and loaded at each 8-bit, i.e., byte-sized, location with image intensity data for first and second images to be blended. Each 8-bits of information represent image information as to first and second pixels, with the intensity level information as to each of the indicated pixels being contained in four bits of information, according to a preferred version of the invention. With these four bits, 16 different gray scales or color intensity levels can be expressed. According to another version of the invention, eight bits of information could be used for a single pixel to represent 256 different gray scale or color intensity levels. However, this would require a much bigger look-up table, which may be unacceptable for many applications according to the current state of the technology. However, for some current applications and as the technology develops, larger look-up tables may become desirable. Actual blending operation is conducted on a pixel-by-pixel basis with reference to use of a color look-up table 360. Loading of buffers 308 and 310 is accomplished at selected times as to the entire contents of buffers 308 and 310. More frequently, only one of VRAM buffers 308, 310 is subject to modification, either, for example, by a selected applications program loading a new image into one of VRAM buffers, for blending operation, or, alternatively, by the user making a change in a selected image entered into the other of the two VRAM buffers 308, 310.

Detailed Description Text (21):
FIG. 8a illustrates a memory map for video and CSC information which can be used with respect to presentation of pixel information on the computer screen, according to the prior art. In particular, FIG. 8a shows a memory region 352 associated with the CPU. Memory region 352 includes subregions 354 and 356 respectively allocated to first video information as to a particular image and also information specific to CSC operation in making pixel frame presentations to the computer display, as will be seen. In particular, video space 354 includes CPU memory locations $6000 0000 to $6FFF FFFF. CSC memory space 356 extends from memory locations $5002 0000 to memory location $5002 IFFF. The corresponding video (i.e., VRAM) buffer locations extend from $6000 0000 to $6007 FFFF. The entire amount of video information is provided to video buffer hardware, in this case to VRAMs 308 and 310, as seen in FIG. 8a. The CSC information is provided to other, selected staggered memory locations within CSC chip 307. Control

over placement of image information at selected memory locations is managed by CPU 12 and memory decoder 19, as suggested in FIG. 1, and as would be understood by one skilled in the art.

Detailed Description Text (22):
FIG. 8b illustrates a memory map for image and CSC information according to the present invention, wherein the CPU has direct control over the placement of image information in VRAM buffers. As in FIG. 8a, memory region 352 includes subregions 354 and 356 respectively allocated to first image information as to a particular image and also information specific to CSC operation in making pixel frame presentations to the computer display. However, according to one version of the invention, the image information comes in two kinds, first image information as to a base image, and second image information as to an overlay image. Accordingly, the information may be segregated in any one of a number of ways. According to one version, all of the first image information, i.e., that dealing with the base image, can be allocated to VRAM buffer 310. Concomitantly, all of the second image information, i.e., that dealing with the overlay image, can be allocated to the other VRAM buffer 308. Other variations are workable as well. For example, the first and second images can be interspersed within the VRAM buffers 308 and 310, so long as they are organized suitably to be available pixel-by-pixel (or by pixel pairs) for blending operation and presentation on the computer display as part of an image frame.

Detailed Description Text (23):
FIG. 9 illustrates features of CSC chip 307 including a color look-up table (CLUT) 360, data formatter 362, VRAM controller 364, and CPU interface 366. According to a preferred version of the invention, the color look-up table 360 controls the color in pixels within a selected frame being displayed on a computer screen. Further according to the invention, color look-up table 360 is addressed by an 16 bit line from VRAM buffers 308, 310. This 16 bit line permits addressing of 256 locations on color look-up table 360 as to first and second pixels. Color look-up table 310 can accordingly permit reference to a broad number of pixel colors for presentation to the computer screen viewer. If the computer screen is black and white and permits the presentation of gray scale images, these various desired levels of gray can conveniently be represented in order appropriately to drive the computer display. Depending upon whether an analog or digital signal is desired from the look-up table, the output of the look-up table 310 can be channeled appropriately through data formatter 362 directly to LCD control and data ports of the external display assembly for presentation on a computer screen or monitor, as would be understood by one skilled in the art. VRAM controller 364 is effective for calling appropriate pixel locations in VRAM buffers 308 and 310 for application to color look-up table 360 along line 311.

Detailed Description Text (25):
Thus, according to the invention, there is a mechanism for blending first image data and second image data to produce a blended image on the screen assembly by first storing image and overlay information in VRAM buffers 308 and 310, combining pixel amounts thereof in blending operation, and addressing a preestablished look-up table 360 in display driver 21 in order to establish the character of single pixel presentation on computer screen 60 in accordance with the results of blending operation. The VRAM buffers 308, 310 are loaded by applying selected bit amounts of first image information about selected, successive pixels "A" and "B" in separate VRAM buffers, such that the first image information about pixel "A" is entered in one of the VRAM buffers and the first image information about pixel "B" is entered in the other one of the VRAM buffers. Next, the second image information about pixels "B" and "A" is loaded onto the same respective, separate ones of VRAM buffers 308 and 310. As a result of this scheduling, the first image information on a particular pixel is in one of the VRAM buffers 308, 310 and the corresponding second image information, i.e., the overlay information, is in the other VRAM buffer. Further, according to the invention, all the data on a particular pixel is provided for blending operation by addressing both of the VRAM buffers 308, 310 to produce complete image and overlay information about a particular pixel concurrently. After completion of blending operation, the display driver 21 is called for addressing a color or gray scale look up table 360. The color look-up table 360 is a preferred version of the invention in which the color look-up table 360 controls the color in pixels within a selected frame being displayed on computer screen 60. According to an alternate embodiment of the invention, gray scale information is selected by the blending output to produce frame pixel information for presentation on computer screen 60.

Detailed Description Text (26):
In summary, the circuitry according to the invention herein, and as explained with

reference to FIGS. 7, 8a, 8b, 9, and 10 permits the receipt along data bus 28 of image information as to first and second images to be blended. The image information is accompanied by address information which identifies data on data bus 28 as belonging either to the first or the second image. Further, a selected bit line of address bus 31 is selected to provide an indication as to whether a particular data item belongs to the first or the second image. According to one version, address line A(20) is assigned to identify the particular image. The data identified is applied to either VRAM buffer 308 or VRAM buffer 310, depending upon the state of address line A(20). For example, if the state of address line A(20) is "1," then the data from data bus 28 is provided to VRAM buffer 308. Alternatively, if the state of address line A(20) is "0," the data from data bus 28 is provided to VRAM buffer 310. More particularly, the data from data bus 28 is connected along data lines D(31:24) to both of VRAM buffers 308 and 310. Each of VRAM buffers 308 and 310 is connected to a select line from VRAM select logic circuit 311. According to one version, VRAM select logic circuit 311 selects VRAM buffer 308, if the input to VRAM select logic circuit 311 is a "1" along address line A(20). If the input to VRAM select logic circuit 311 is a "0" along address line A(20), then VRAM select logic circuit 311 is effective for selecting VRAM buffer 310. Thus, while data lines D(31:24) are connected to both VRAM buffers 308 and 310, data from data lines D(31:24) will be input only into the selected one of VRAM buffers 308 and 310. The actual data provided according to one version comes in eight bit amounts. These eight bits can represent data as to a single pixel or according to a preferred version, the first four bits represent image data as to a first pixel and the next four bits represent data as to a next pixel. Four bits are sufficient to represent 16 levels or shades of intensity in terms of color or grayness as to a particular pixel. Eight bits, however, can represent 256 levels or shades of color or grayness. The output of VRAM buffers 308 and 310 is provided in terms of eight bits from each VRAM buffer. For example, VRAM buffer 308 provides eight bits of output data along lines SD(31:28) and SD(23:20), and VRAM buffer 310 provides eight bits of output data along lines SD(27:24) and SD(19:16). These data lines are combined as a single bus including lines SD(31:16). Lines SD(23:16) represent the blending of data from lines SD(23:20) from the image data of a first image stored in VRAM buffer 308 and data from lines SD(19:16) from the image data of a second image stored in VRAM buffer 310. Lines SD(31:24) represent the blending of data from lines SD(31:28) from the image data of a first image stored in VRAM buffer 308 as to a next pixel and data from lines SD(27:24). In this fashion, data is loaded into and extracted from VRAM buffers 308 an 310 in order to accomplish blending of two images.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 3. Document ID: US 5321828 A

L4: Entry 3 of 4 File: USPT Jun 14, 1994

DOCUMENT-IDENTIFIER: US 5321828 A
TITLE: High speed microcomputer in-circuit emulator

Detailed Description Text (82):
Shadow memory 60 allows the external ICE to interface to the BUS 24. There are many uses of the shadow memory 60. In mode 66, the shadow memory 60 is used as a temporary storage buffer between the external ICE and target microprocessor 26. In command mode, the shadow memory 60 is used to store user programs. In ICE 10 design, the shadow memory 60, along with the PC/AT 20, assists in sending mode 66 commands. The shadow memory 60 section comprises the following subsections:

Detailed Description Text (760):
DATA clears one or both data breakpoints internal to the Intel i960 CA chip.

Detailed Description Text (773):
DATA clears the range breakpoint on the target system 14 data bus.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 4. Document ID: US 4104629 A

L4: Entry 4 of 4 File: USPT Aug 1, 1978

DOCUMENT-IDENTIFIER: US 4104629 A
TITLE: Marine radar interrogator-transponder target detection, identification, and range measurement system

Detailed Description Text (215):
The structure of the input memory system is similar, but in the drawing, certain stages are broken apart because signals must be processed between those certain stages. There is a vertical memory section including sub-sections 813a, 823a, 831a, and 832a which again comprises twelve shift registers, each having a total of four stages and arranged in parallel connection with respective 12-conductor leads such as at 825, 831 and 815. This vertical memory section again holds address data. Memory section 813b, 823b, 831b, 832b is similar to memory section 813a, 823a, 831a, 832a, but has 13 four-stage registers cooperating with respective 13 conductor leads such as lead 829, 822, 816. This section stores range data that, along with the address data, has not been placed in the desired order. Similarly, disordered data in the form of a single bit resides in a single shift register whose four sections include sections 813c, 823c 831c 832c, as will be further described. Shift and other control signal leads are again supplied for all shift registers in the usual manner. It will be understood that the row designations A1, B1, C1, D1, and A2, B2, C2, D2 correspond to the locations of the successive stages of the 26 shift registers used in this example.

Detailed Description Text (260):
At the same time, the coincidence pulse from comparator 812 is fed both via lead 812b to set flip flop 929 and via OR gate 928 to set flip flop 925. The now-high one output of flip flop 929 will illuminate the two-targets-with-the-same-address display element 931 via amplifier 930. The now-high one output of flip flop 925 enables the analog AND gate 926, permitting a driving signal, for example of 1000 Hz frequency, to pass from a suitable source (not shown) attached to terminal 926a to drive the alarm speaker 927. The alarm speaker 927 may be silenced at the convenience of the operator upon touching the silencing key 924 which resets flip flop 925, thereby inhibiting AND gate 926. When the operator completes a conclusive conversation over own ship's radio telephone with the other vessel or vessels, he can clear the two-with-the-same-address light by depressing any enter key in the group 154. Whenever the operator touches a C'DPA data entry key, decoders 933 and 943 put out a high level signal on a corresponding output line. Therefore, to clear particular C'DPA data from one of the readouts, the operator first touches the C'DPA data entry key and then touches the clear C'DPA data key 923. It will, of course, be understood that the other latches and corresponding displays will normally be used consecutively and that they operate in the same manner as has been discussed in connection with latch 936a and readout 934a.

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